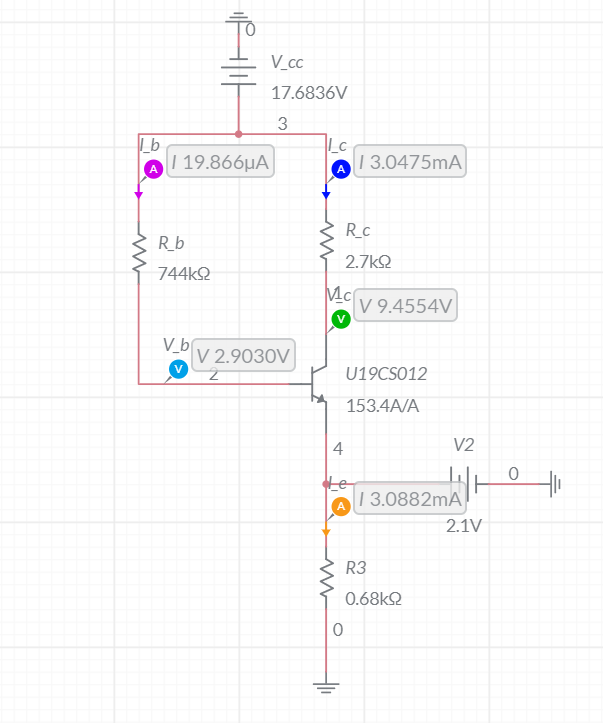
**ASSIGNMENT-10**

U19CS012

1.) Using the information provided in the figure below, determine the values of Beta, Vcc and Rb theoretically. Also compute and verify the values of Ic, Vb, and Vc by implementing the circuit on Multisim.



*1.) Circuit Image:*



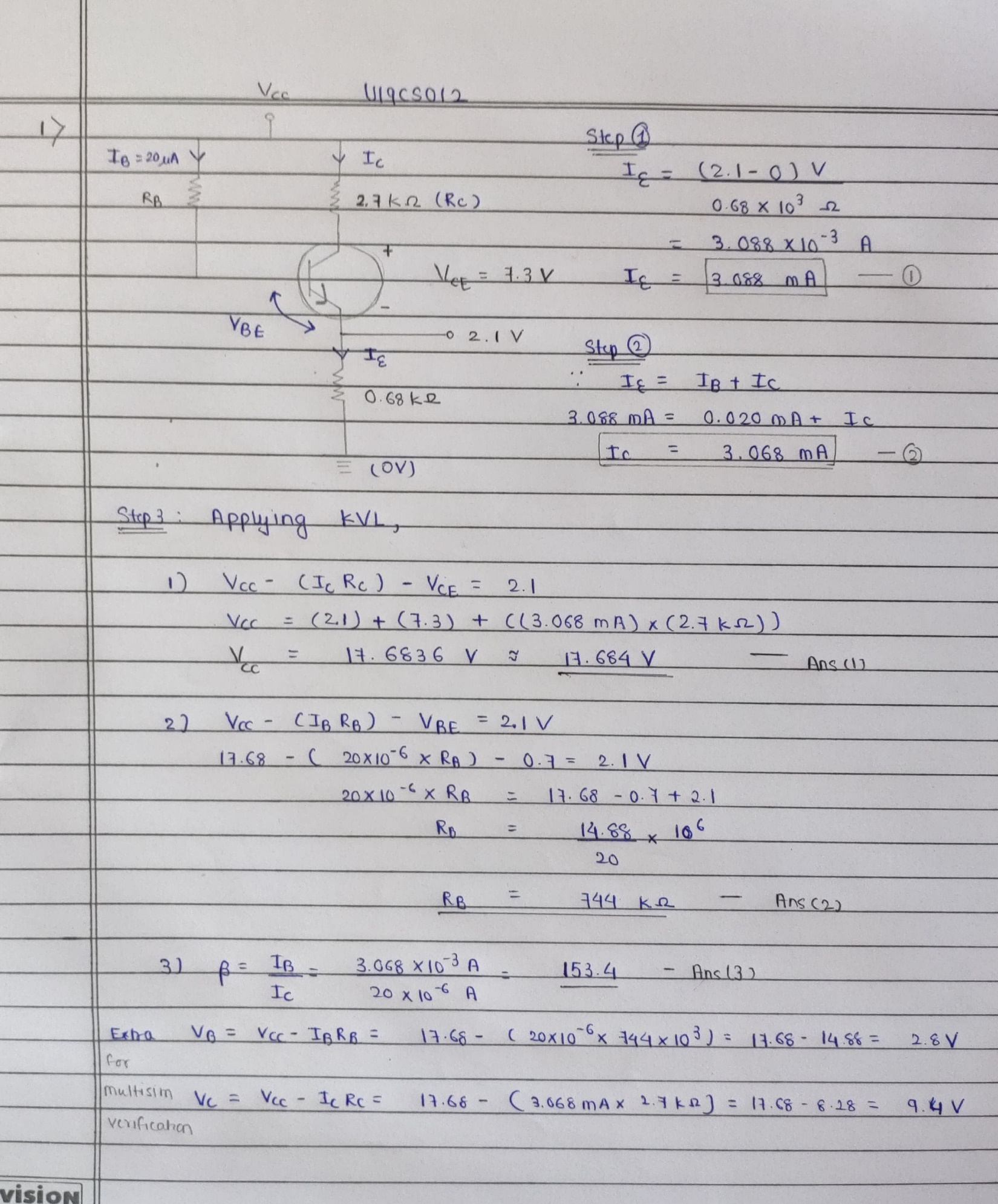
*2.) Grapher Image:*



|  |  |  |
| --- | --- | --- |
| **Parameter** | **Graph** | **Theoretical** |
| Vb | 2.9030 V | 2.8 V |
| Vc | 9.4554 V | 9.4 V |
| Ib | 0.019866 mA | 0.020 mA |
| Ic | 3.0475 mA | 3.068 mA |
| Ie | 3.0882 mA | 3.088 mA |

We can Clearly See Both the **Theoretical** and **Multisim Values** are *Approximately Equal*. Hence the Experiment was Performed Successfully and Circuit is verified.

*3.) Calculations*

**

**2.** Simulate the below given circuit on Multisim and predict the type of Digital Logic implemented by the same. Use the default transistor available in Multisim. Attach all the four screenshots (00, 05, 50 and 55).



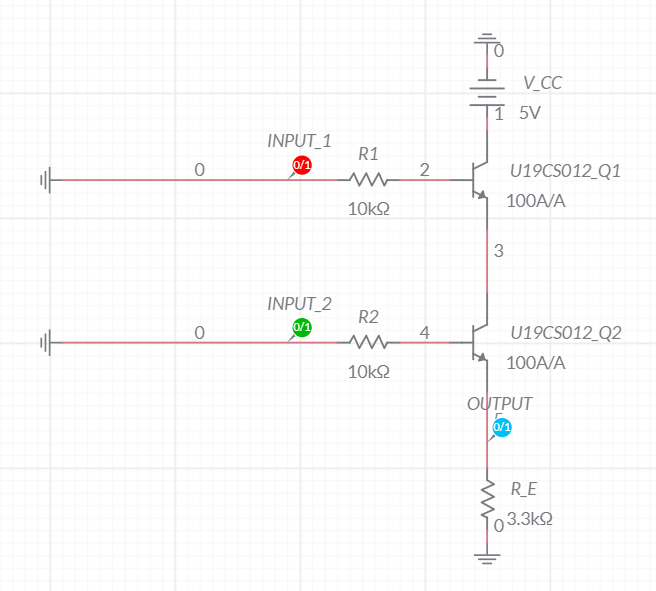
Answer:

By Observing the Truth Table Obtained from Multisim Simulation, We can clearly see that the Above Circuit [Equivalent to] represents the **Logical AND** Gate.

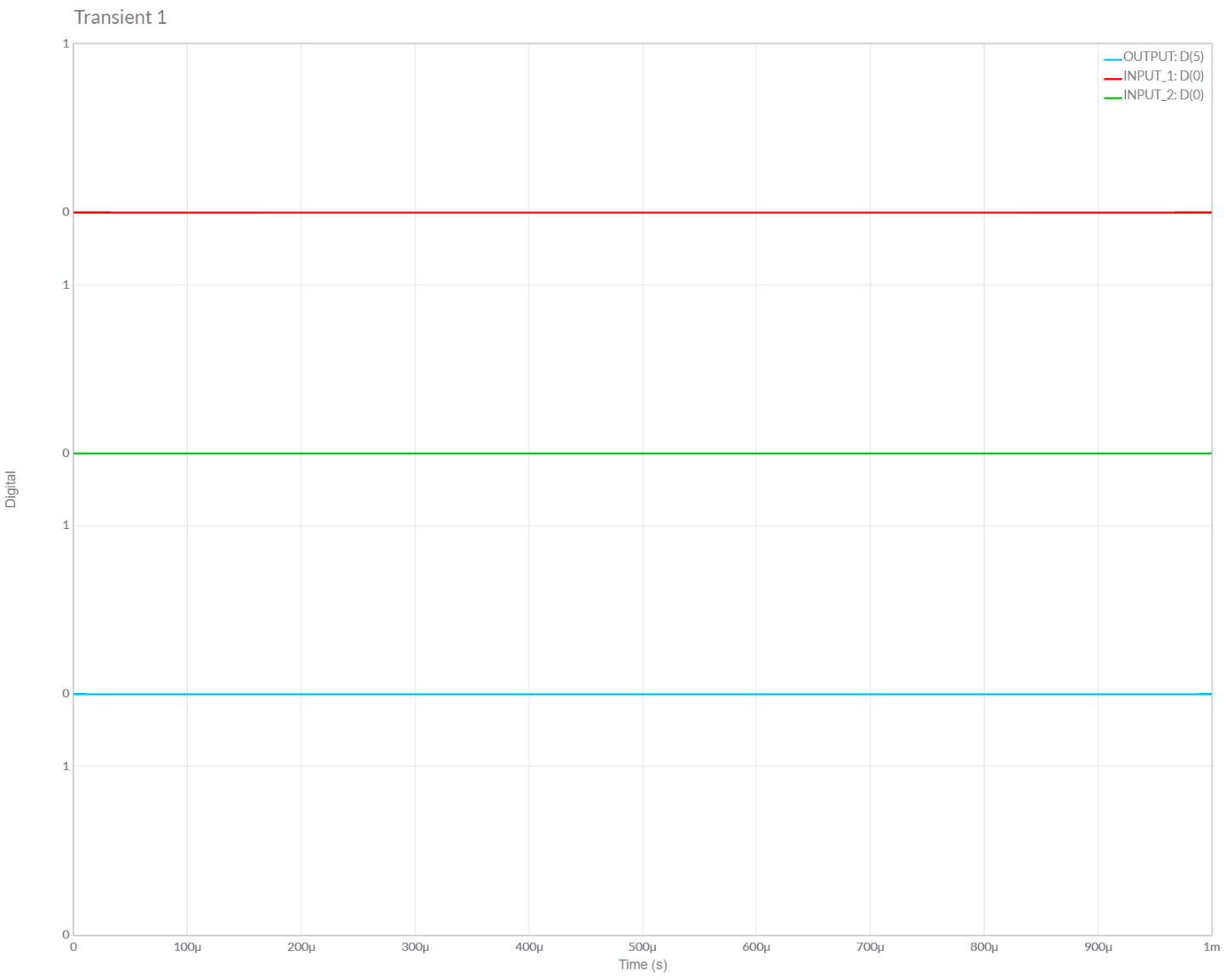
|  |  |  |
| --- | --- | --- |
| **INPUT1** | **INPUT2** | **OUTPUT** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

A.) Case #1: 00

*1.) Circuit Image:*

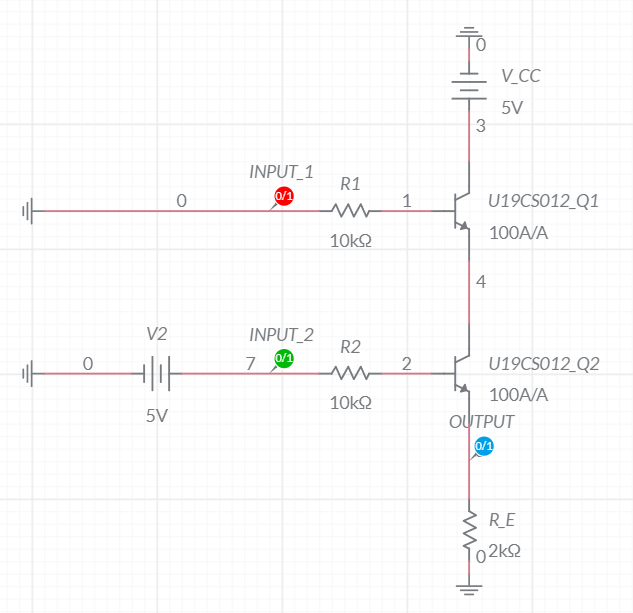


*2.) Grapher Image:*

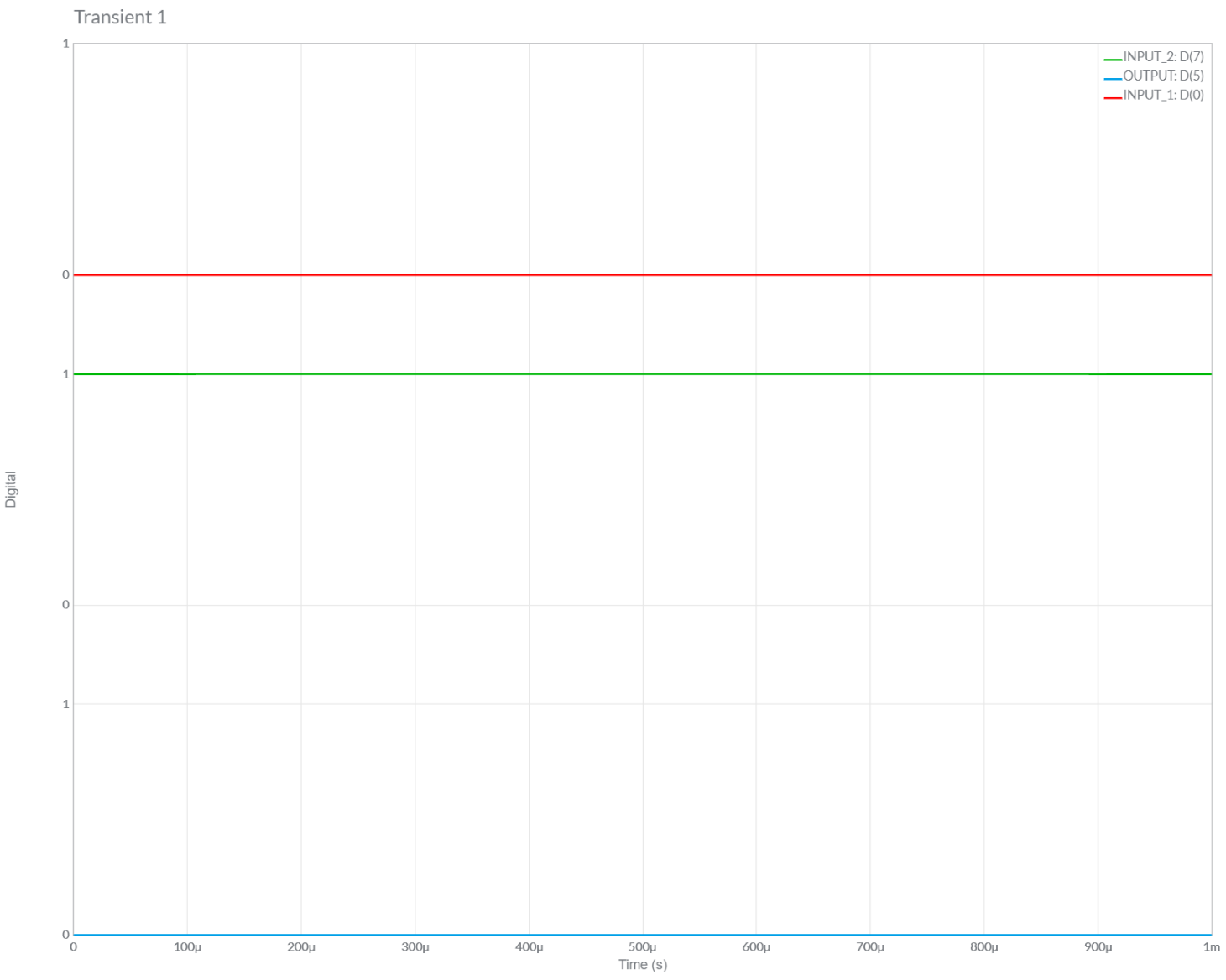
**

B.) Case #2: 05

*1.) Circuit Image:*

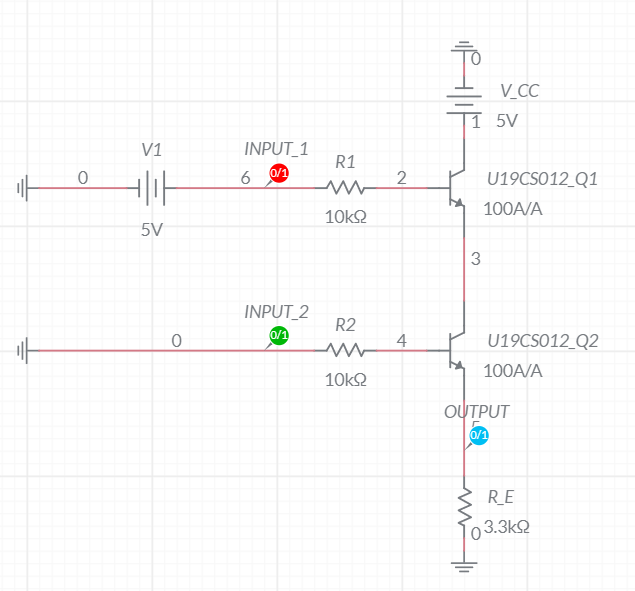


*2.) Grapher Image:*

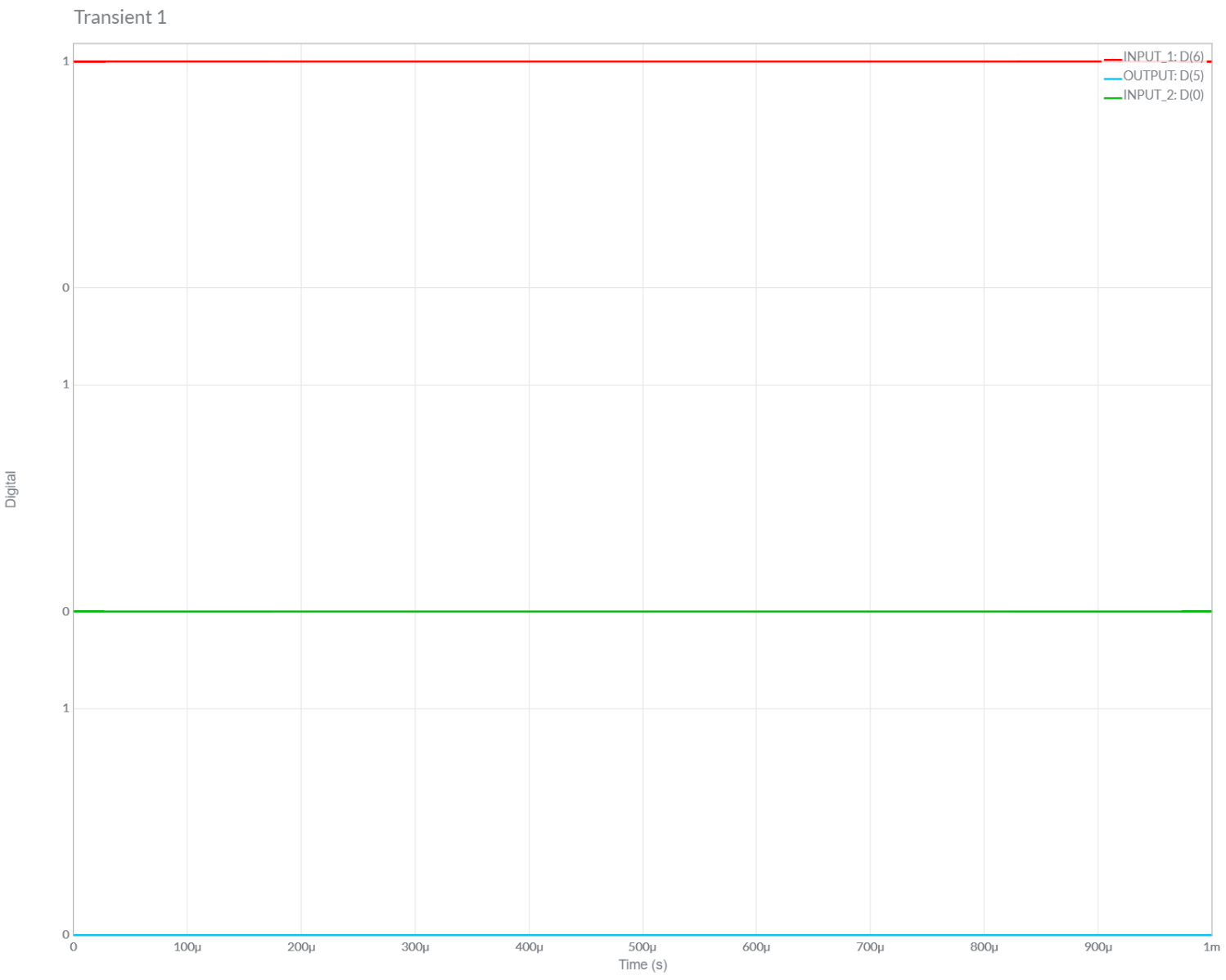
**

C.) Case #3: 50

*1.) Circuit Image:*

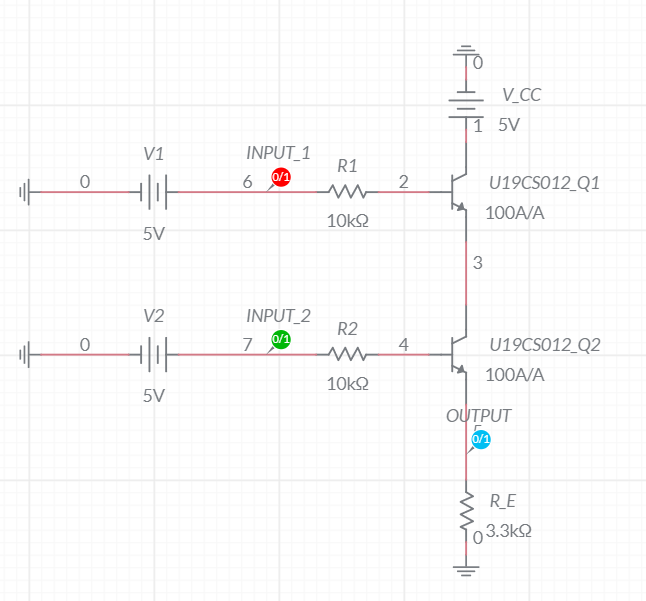


*2.) Grapher Image:*

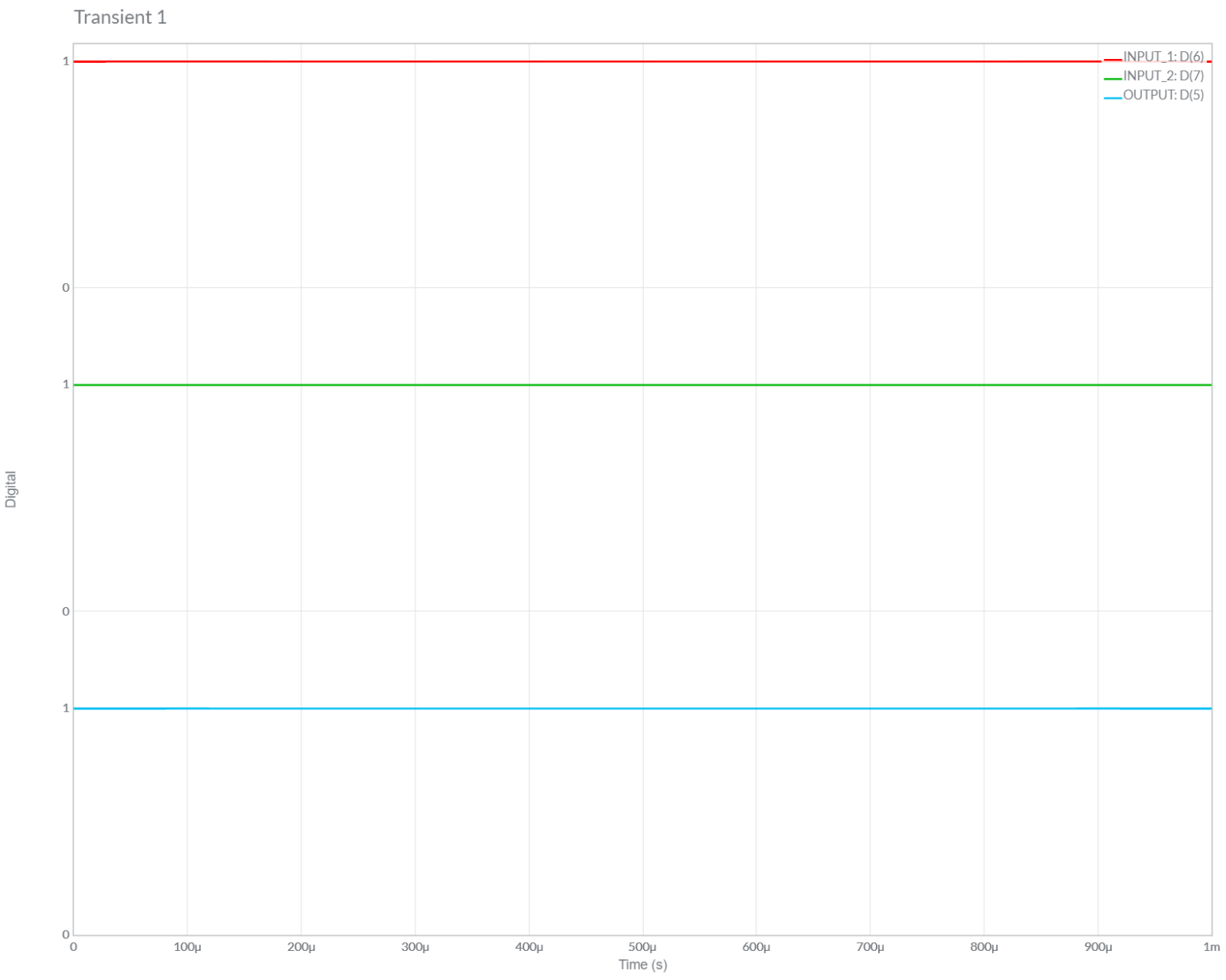
**

D.) Case #4: 55

*1.) Circuit Image:*



*2.) Grapher Image:*

**